FPGA Implementation of a Fuzzy Rule Based Contrast Enhancement System for Real Time Applications

Tigaeru Liviu
Faculty of Electronics, Telecommunications and Information Technology
Technical University Gheorghe Asachi
Iasi, Romania
ltigaeru@etti.tuiasi.ro

***Abstract* - The present paper describes a pipeline digital architecture of a fuzzy rule base grayscale image contrast enhancement system. The proposed system uses a zero order Takagi-Sugeno fuzzy model, adapted to avoid the division operation in the deffuzification block and also to reduce the computational requirements for the fuzzification block. The digital architecture is optimized to benefit from the advantages provided by the Xilinx DSP48E2 slice in terms of speed and logic resource consumption. The design has been synthesized and tested on a Xilinx FPGA device and the reported results confirm its viability to be embedded in real time application systems. Also, the functionality of the proposed system was tested on a set of low contrast images, illustrating heavy traffic conditions.**

Keywords — grayscale image contrast enhancement, fuzzy logic, fuzzy contrast enhancement, FPGA design, DSP48 slice

I. INTRODUCTION

Image processing and computer vision are important research areas, with contributions in a lot of emerging applications, as autonomous vehicles, driver assitance systems, visual surveillance systems, assisting humans in identification tasks, medical computer vision or medical image processing systems, etc. In real environments, the images are considerably altered by insufficient lighting sources, improper focusing or heavy environment conditions, during the image acquisition process, etc. that lead to noisy, poor in contrast, nonuniform illumination images. Various algorithms for image enhancement have been proposed, some of them aims on noise removal, others operate on the gray-level dynamic range to improve the quality of the image. Among them, contrast enhancement is one of the most important technique, applied to digital images to improve or even brings out various details contained in the original image, with many applications in computer vision and pattern recognition fields. Numerous contrast enhancement solution have been published during years. A lot of them are based on histogram equalization procedure [1], a computationally fast and simple to implement solution, but causing significant changes of the brightness of the image, which generate annoying intensity saturation effects. Therefore, several improvements of the classical histogram equalization technique were reported, that bring in various solutions that preserve the brightness of the initial image. One of the main improvement is the bi-histogram equalization technique [2], based on the independent equalization of two sub-histograms derived from the original histogram, based on the mean brightness point of the input image. Similar solutions are described in [3] and [4], where the median of brightness and optimal brightness point of the input image are used instead of the mean brightness respectively, to partition the original histogram. In the latter case, the optimal brightness point is determined based on an algorithm that finds the minimum mean brightness error between the original and the enhanced image. Other variations are the techniques that treat differentially distinct areas of the original image. These techniques [5, 6, 7, 8] equalize several histograms, each corresponding to a distinct area of the image.

Other approach in contrast enhancement techniques are based on fuzzy sets theory [9] used as a tool for handling the uncertainty present in the images. The motivation behind this is the imprecise definition of the concept of image contrast and also the vagueness occurred in the processed image, caused by the uncontrollable variables specific to the image acquisition process. Early fuzzy logic based contrast enhancement solutions were based on the contrast intensification (INT) operator [10] and the later improved new intensification operator (NINT) [11], to change the dynamic range of the image, according to a membership degree which depends on a threshold value.

An often used method is the fuzzy logic based histogram equalization technique that enhances the image contrast while preserving the brightness of the original image. This technique maps the input image from the space domain to the fuzzy domain, based on a membership function and then applies a fuzzy contrast enhancement algorithm, to improve the image quality in terms of contrast [12, 13]. Some of these solutions are based on fuzzy measures of the information contained in the processed image, as entropy of the image [14], parametric indices of fuzziness [15], or fuzzy intensity measure [16], used as optimization criterions of the contrast enhancement procedure.

Other fuzzy logic based contrast enhancement approach uses fuzzy rule based techniques [17, 18, 19], where the

978-1-5386-4444-7/18/$31.00 ©2018 IEEE

human knowledge about the concerned problem to solve plays an important role in making decisions. In image contrast enhancement applications, the incorporation of the human intuition about the processed image can be beneficial, leading to well-balanced output images that preserves the brightness of the original image while brings-out the hidden details, or improves the contrast. In spite of its benefits, this method suffers from high computational time, making it unsuitable to be implemented in real time applications. The challenges raised by this method can be solved by hardware implementations, by their inherent computational speed. In this regard, FPGA based implementation of the fuzzy systems proved to be very effective solutions [20, 21, 22]. This issue motivated the current work, where the main goal was to design a digital architecture for an image contrast enhancement system, optimized for DSP logic resources, integrated in the latest FPGA devices. During this process, one important concern was to develop a solution suitable to be embedded in a visual system, serving real time applications.

Even the present paper proposes a digital architecture tailored for the Xilinx DSP48E2 slice, the solution can be adapted to match other similar DSP logic resources, integrated in various current FPGA devices.

The remainder of this paper is organized as follows. The fuzzy model is presented in Section 2, emphasizing the introduced constraints that simplify the fuzzification and defuzzification blocks, respectively. Section 3 describes the digital architecture of the proposed contrast enhancement system, underlying the optimization technique for an efficient Xilinx DSP48 slice based implementation. The FPGA implementation result and the test of the functionality of the proposed system respectively are addressed in Section 4. Finally, Section 5 draws some conclusions.

II. THE FUZZY MODEL

The proposed contrast enhancement system is based on a zero order Takagi Sugeno fuzzy model [23], shown in Fig. 1. The model has an input fuzzy variable, denoted by *input_pixel*, where the pixel of the input image is supplied and an output variable, denoted by *output_pixel*, that provides the enhanced pixel. Both fuzzy variables are defined over the universe of discourse [0, 255], set by the range of the gray levels of the processed image.

Five trapezoidal/triangular input fuzzy sets are defined, while the output fuzzy sets are singletons, as are depicted in Fig. 2. The specific shapes of the input fuzzy sets and the singleton values of the output fuzzy set, respectively, depend on the transformation function, required to enhance the contrast of the input image. However, for the inner input fuzzy sets, only triangular shaped fuzzy sets are chosen to avoid introducing plateaus into the transformation function generated by the fuzzy model, since these does not not contribute substantially to the contrast enhancement.

All input fuzzy sets are defined by means of the set of peak parameters, denoted by p_k, k = 0,4 where $p_0 > 0$, $p_{k-1} < p_k$, $p_4 < 255$, are satisfied respectively.

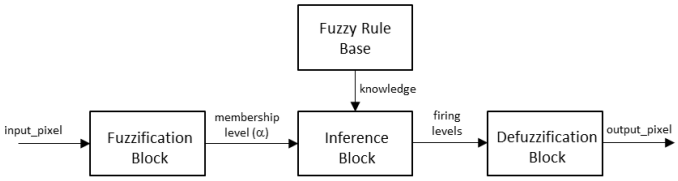

Fig.1. The structure of the fuzzy model

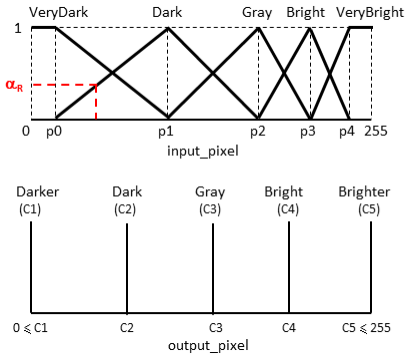

Fig.2 The fuzzy sets of the fuzzy model

The fuzzy model is composed of 4 distinct blocks: a fuzzification block, which takes the crisp values of the *input_pixel* and transforms it into degrees of membership (alpha values) to the defined input fuzzy sets, which are used to express the linguistic values, a rulebase containing a number of fuzzy rules expressed as in the table below, which describes the expert knowledge about the considered problem to solve, an inference block which computes, using the product operator, the firing levels of the fuzzy rules and a defuzzification block, which aggregates the contributions of all active fuzzy rules into a new crisp value of the *output_pixel* variable.

TABLE I. FUZZY RULEBASE

IF INPUT_PIXEL IS	VERYDARK	THEN	OUTPUT_PIXEL = DARKER
IF INPUT _PIXEL IS	DARK	THEN	OUTPUT_PIXEL = DARK
IF INPUT _PIXEL IS	GRAY	THEN	OUTPUT_PIXEL = GRAY
IF INPUT _PIXEL IS	BRIGHT	THEN	OUTPUT_PIXEL = BRIGHT
IF INPUT _PIXEL IS	VERYBRIGHT	THEN	OUTPUT_PIXEL = BRIGHTER

In order to simplify the hardware implementation of the fuzzy model, normalized fuzzy sets, that generate a fuzzy partition over their universe of discourse, are used for the input fuzzy variable. Since in a fuzzy partition at most two adjacent fuzzy sets are simultaneously active, only at most two membership degrees, denoted by α_L and α_R have nonzero values. Also, since at most two fuzzy sets are simultaneously active, at most two fuzzy rules are active at the same time, contributing to the output value. Besides, due to the normalization property, the relation $\alpha_L = 1 - \alpha_R$ is always available. Finally, due to these constraints, the output value of the fuzzy model can be calculated as in (1), avoiding the division operator in the deffuzification block and also the necessity to calculate α_L membership degree:

$$output\_pixel = \frac{\alpha_L \cdot c_L + \alpha_R \cdot c_R}{\alpha_L + \alpha_R} = \frac{(1-\alpha_R)\cdot c_L + \alpha_R \cdot c_R}{1-\alpha_R + \alpha_R}$$

$$output\_pixel = \alpha_R \cdot (c_R - c_L) + c_L \quad (1)$$

The membership degree of the used fuzzy model can be calculated as

$$\alpha_R = \begin{cases} m \cdot input\_pixel - n & input\_pixel \in [p0, p4] \\ 1 & otherwise \end{cases} \quad (2)$$

where m and n are two parameters whose values depend on the relation between the *input_pixel* value and the intervals defined by the difference between two successive peak values, $p_k - p_{k-1}$,

$$m_k = \frac{1}{p_k - p_{k-1}} \quad n_k = \frac{p_{k-1}}{p_k - p_{k-1}} \quad k = 1,4$$

III. THE DIGITAL ARCHITECTURE OF THE FUZZY MODEL

The digital architecture of the fuzzy model is designed such that to exploit the capabilities provided by the optimized DSP blocks, integrated in current FPGA devices. The solution used to design the digital architecture is tailored to benefit from the advantages provided by the DSP48 slice, integrated in the latest Xilinx FPGA devices, as UltraScale device families, etc., in terms of speed and logic resource consumption.

A. DSP48E2 slice

Even the current work uses as logic support to implement the proposed fuzzy model, the Xilinx DSP48E2 slice [24], similar solutions can be adapted to other DSP blocks, provided by others FPGA device vendors.

The simplified structure of the DSP48E2 slice is given in Fig.3. It has four inputs of different wordlengths: 30, 18, 48, and 25 bits, respectively and a set of arithmetic sub-blocks and registers, that can be combined to implements different pipelined arithmetic or logic functions. The DSP48E2 slice consists of a 27-bit preadder, which can operates as an add/subtract unit, a 27x18 two's complement multiplier which can be is used in a multiply and accumulate structure and a flexible 48-bit ALU block that can operates as a post-adder/subtracter or logic unit.

B. The Digital Architecture

In order to obtain an effective FPGA implementation of the proposed fuzzy model, its digital architecture was optimized taken into account the logic resources provided by the DSP48E2 slice. Thus, using the recommended design flow, the DSP48E2 resources are well suited to implement the equations that describe the proposed fuzzy model.

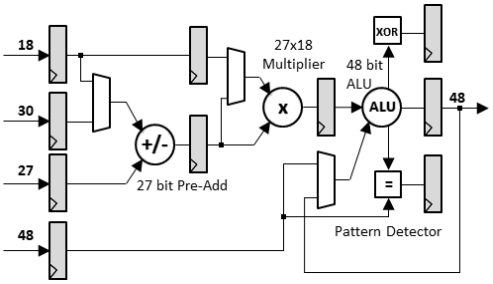

Fig.3. The simplified structure of the DS48E2 slice

Since the proposed system for image contrast enhancement uses only 8 bits grayscale images, all values related to the pixels are represented on 8 bits. This implies that input pixel, output pixel, p_k peak parameters and also the consequences of the fuzzy rules are all represented as integers on 8 bits. On the other hand, m, n parameters are represented as fixed point numbers on 18 bits (S.17 format) and 27 bits (SS.8.17 format), respectively, where S stands for the sign bit, which is always equal to 0 for both parameters. The format choice of these parameters was adopted based on the dimension of the input signals of the DSP48E2 slice.

The architecture of the fuzzy model is presented in Fig. 4. and consists of three main blocks:

- the *range_detector* block compares the input pixel value with the peak parameters p_k, identifies the interval $[p_k, p_{k-1}]$, k = 1,4 where the input pixel belongs to and outputs this information as a binary code;
- the *active_rule_detector* block takes the information about the range where the input pixel belongs to and find the active fuzzy rules from the fuzzy rulebase, delivering the corresponding consequences and also the corresponding m, n parameters, required for the membership degree calculation; the possible output values of the *active_rule_detector*, depending on the range where the input pixel belongs to, are summarized in Table II.

TABLE II. THE SELECTION OF THE ACTIVE FUZZY RULE PARAMETERS

pixel range	m	n	c_L	c_R
input_pixel ∈ [0, p0]	0	0	c1	0
input_pixel ∈ (p0, p1]	m1	n1	c1	c2
input_pixel ∈ (p1, p2]	m2	n2	c2	c3
input_pixel ∈ (p2, p3]	m3	n3	c3	c4
input_pixel ∈ (p3, p4]	m4	n4	c4	c5
input_pixel ∈ (p4, 255]	0	0	c5	0

- the *fuzzy_core* block is broadly responsible for the implementation of the fuzzy model; it takes the input pixel value and compute the output pixel according to the fuzzy model, based on the consequences of the active fuzzy rules and the corresponding m, n parameters.

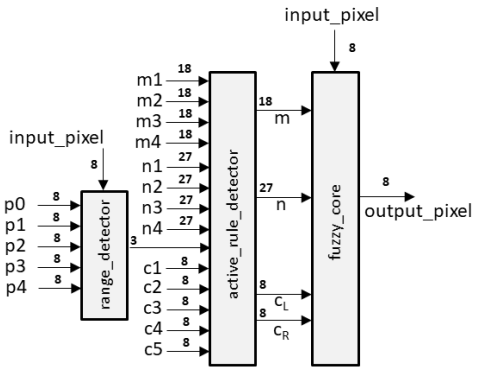

Fig. 4 The digital architecture of the fuzzy model

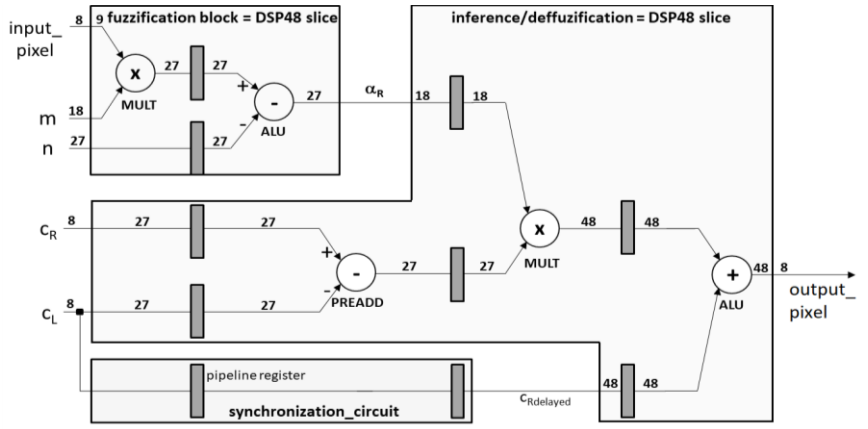

Fig. 5. The structure of the fuzzy core block

The digital architecture of the fuzzy model is based on a pipelined fuzzy core structure. Its structure, shown in Fig.5, is optimized to consume only two DSP48E2 slices and consists of a fuzzification block and an inference-deffuzification block, both tailored to consume each a single DSP48E2 slice and a synchronization block, respectively. The fuzzification block implements the equation (2); it takes the input pixel and computes its membership degree α_R, depending on the corresponding *m*, *n* parameters. Subsequently, the value of the membership degree, truncated to 18 bits to match the DSP48E2 slice resources, is taken by the inference/defuzzfication block, that implements the equation (1), in order to compute the value of the output pixel, based on the consequences of the active fuzzy rules.

IV. IMPLEMENTATION AND RESULTS

The proposed architecture was implemented on a Xilinx Kintex UltraScale FPGA device (xcku035) using Vivado tool, and the obtained results confirm the design expectations. The resource utilization report certify that only two DSP slices are consumed to implement the arithmetic circuits of the fuzzy model, while the rest of logic required 27 LUTs and 16 FlipFlops respectively, validating the efficiency of the proposed solution in terms of logic resource consumption.

The critical paths of the digital architecture are generated by the arithmetic circuits, used to implement the operations specific to the fuzzy model. The optimization of the digital architecture to use DSP slices as logic support for the arithmetic operations assures a significant reduction of the signal delays on these paths. The timing report, generated after the implementation of the digital architecture on the FPGA device, shows a total delay on the critical path of 5.13ns, which allows a fast processing time even for high dimension grayscale images.

To check the functionality of the proposed contrast enhancement system, a set of 256x256 grayscale images, illustrating several defining low visibility traffic conditions, were tested. To have a complete view about the ability of the proposed system to enhance the contrast of the considered images, various lighting or weather traffic condition were considered (night traffic, blizzard traffic, foggy traffic, etc). During the test procedure, each input image was supplied to the proposed system from a ROM memory, were initially it was loaded. The output image, generated by the system, was saved in a RAM memory and also as a text file, then imported in Matlab environment to analyze the obtained results. Fig. 6 shows the results generated by the proposed contrast enhancement system. The leftmost columns provide the test images and their corresponding histograms, the middle column displays the transformation functions generated by the implemented digital architecture of the fuzzy model and the rightmost columns represent the output images along their enhanced histograms. One of the advantages of the fuzzy rule based contrast enhancement systems consists in their ability to adjust the transformation function to the particularities of the histogram shape of the processed image. The obtained results, displayed on the middle column of the Fig. 6. validates this property. As can be noticed, images illustrating various lighting/weather traffic conditions have various histogram shapes. However, modifying the peak set of the fuzzy input sets and the consequences of the fuzzy rules, easily tunes the transformation function generated by the proposed system, to follow the characteristics of the test image in order to enhance its contrast. As can be seen from Fig. 6, the images taken in night traffic conditions are brightened by the proposed system, to reveal unseen obstacles or road details. On the other hand, the images taken in foggy traffic conditions are balanced for a better definition of the traffic partners, to avoid the collision to them. A darken effect can also be seen in the images taken in blizzard traffic conditions, where the traffic partners or other obstacles are located.

V. CONCLUSION

The present paper proposed a fuzzy rule based contrast enhancement system digital architecture, optimized for the Xilinx DSP48E2 slice based implementation. Although the arithmetic core of the digital architecture is tailored to benefit of the advantages in terms of speed and logic resource utilization, given by the DSP48E2 slice, the presented solution can be adjusted for other arithmetic logic resources, provided inside the structure of various FPGA devices.

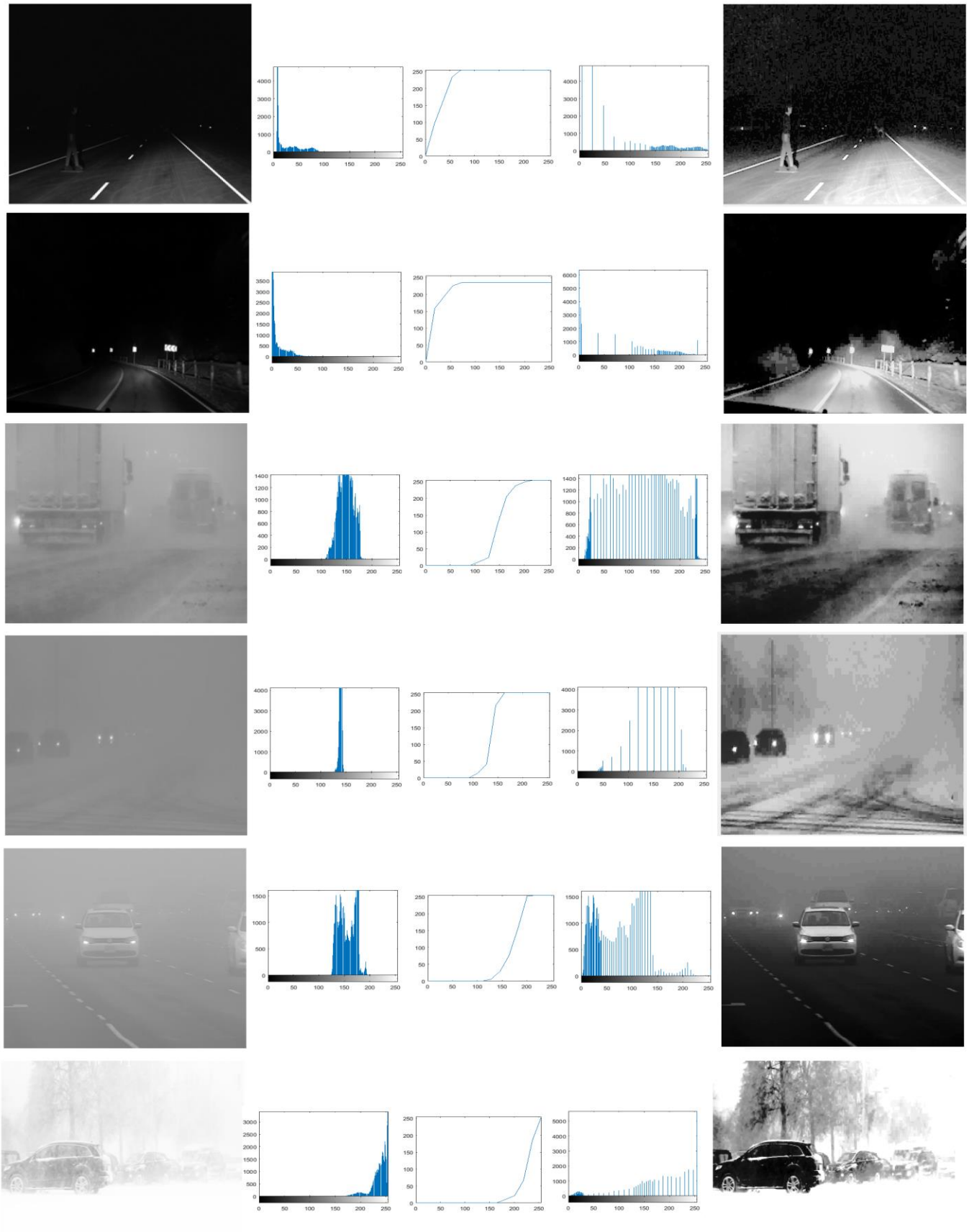

Fig.6. The obtained results for the implemented fuzzy rule based contrast enhancement system

The proposed architecture was implemented on a Xilinx Kintex UltraScale FPGA device and the reported results confirm the efficiency of the proposed solution in terms of logic resource consumption and speed, that validate it for real time applications, as vision systems, etc. Finally, the functionality of the implemented contrast enhancement system was tested on a set of various low contrast images, illustrating different heavy traffic condition. The obtained results prove the versatility of the proposed system to satisfy various challenges raised by the different low contrast images.

REFERENCES

[1] R. C. Gonzalez, R. E. Woods, "Digital Image Processing", 3rd ed., Prentice Hall, 2011

[2] Y.-T. Kim, "Contrast enhancement using brightness preserving bihistogram equalization", IEEE Transactions on Consumer Electronics, vol. 43, no. 1, pp. 1-8, 1997

[3] Y. Wan, Q. Chen, and B.-M. Zhang, "Image enhancement based on equal area dualistic sub-image histogram equalization method," IEEE Transactions on Consumer Electronics, vol. 45, no. 1, pp. 68–75, 1999.

[4] S. D. Chen, A. R. Ramli, "Minimum mean brightness error bi-histogram equalization in contrast enhancement," IEEE Transactions on Consumer Electronics, vol. 49, no. 4, pp. 1310– 1319, 2003

[5] S.M. Pizer, E. P. Amburn, J. D.Austin, R. Cromartie, A. Geselowitz, T. Greer, B. Haar Romeny, J. B. Zimmerman, K. Zuiderveld, ″Adaptive histogram equalization and its variations", Computer Vision, Graphics and Image Processing, vol. 39, no. 3, pp. 355-368, 1987

[6] K. Zuiderveld, "Contrast Limited Adaptive Histograph Equalization." Graphic Gems IV. San Diego: Academic Press Professional, pp. 474–485, 1994.

[7] S. D. Chen, A. R. Ramli, "Contrast enhancement using recursive mean-separate histogram equalization for scalable brightness preservation," IEEE Transactions on Consumer Electronics, vol. 49, no. 4, pp. 1301–1309, 2003

[8] D. Menotti, L.Najman, J. Facon, A. A. Araújo, "Multi-Histogram Equalization Methods for Contrast Enhancement and Brightness Preserving", IEEE Transactions on Consumer Electronics, vol. 53, no. 3, pp. 1186-1194, 2007

[9] L.A. Zadeh, "Fuzzy sets", Information and Control, vol. 8, no.3, pp 338–353 , 1965

[10] L. A. Zadeh, "Outline of a New Approach to the Analysis of Complex Systems and Decision Processes", IEEE Transactions on Systems, Man and Cybernetics, vol.3, pp.28-44, 1973

[11] M. Hanmandlu, D. Jha, R. Sharma, "Color image enhancement by fuzzy intensification", Pattern Recognition Letters, vol. 24, pp. 81-87, 2003

[12] H. R. Tizhoosh, G. Krell, B. Michaelis, "On Fuzzy Enhancement of Megavoltage Images in Radiation Therapy", IEEE Conference on Fuzzy Systems, FUZZ-IEEE'97, Barcelona, Spain, vol. 3, pp. 1399-1404, 1997

[13] D. Sheet, H. Garud, A. Suveer, J. Chatterjee, M. Mahadevappa, "Brightness Preserving Dynamic Fuzzy Histogram Equalization", IEEE Transactions on Consumer Electronics, vol. 56, no. 4, pp. 2475 - 2480, 2010

[14] H.D. Cheng, H. Xu, "A novel fuzzy logic approach to contrast enhancement", Pattern Recognition, vol.33 pp. 809-819, 2000

[15] I. K. Vlachos, G. D. Sergiadis, "Parametric indices of fuzziness for automated image enhancement", Fuzzy Sets and Systems vol. 157, pp. 1126–1138, 2006

[16] K. Hasikin, N. Ashidi Mat Isa, "Adaptive fuzzy intensity measure enhancement technique for non-uniform illumination and low-contrast images", Signal, Image and Video Processing, vol. 9, no. 6, pp. 1419–1442, 2015

[17] C. Young Sik, R. Krishnapuram, "A robust approach to image enhancement based on fuzzy logic", IEEE Transactions on Image Processing, vol. 6, pp. 808-825, 1997.

[18] A. Khunteta, D. Ghosh Ribhu, "Fuzzy rule-based image exposure level estimation and adaptive gamma correction for contrast enhancement in dark images", Proceedings of IEEE 11th International Conference on Signal Processing (ICSP), 2012.

[19] V.L. Jaya, R. Gopikakumari, "Fuzzy Rule Based Enhancement in the SMRT Domain for Low Contrast Images", Procedia Computer Science, vol. 46, pp. 1747-1753, 2015

[20] D. Kim, "An implementation of fuzzy logic controller on the reconfigurable fpga system," IEEE Transactions on Industrial Electronics, vol. 47, no.6, pp. 703–715, 2000.

[21] A. Barriga, S. Sanchez-Solano, P. Brox, A. Cabrera, I. Baturone, "Modelling and implementation of fuzzy systems based on VHDL", International Journal of Approximate Reasoning, vol. 41, pp. 164–178, 2006

[22] S. Sánchez-Solano, A. J. Cabrera, I. Baturone, F. J. Moreno-Velo, M. Brox, "FPGA Implementation of Embedded Fuzzy Controllers for Robotic Applications", IEEE Transactions on Industrial Electronics, vol. 54, no.4, pp. 1937-1945, 2007.

[23] T. Takagi, M. Sugeno, "Fuzzy identification of systems and its applications to modeling and control", IEEE Transactions on System Man Cybernetics, vol. 15, pp. 116-132, 1985

[24] Xilinx, "UltraScale Architecture DSP Slice User Guide, www.xilinx.com, 2018